AMENDMENTS TO THE SPECIFICATION

After the Title, insert a paragraph to read as follows:

This is a continuation of U.S. Patent application No. 10/121,790, filed April 10, 2002, and is related to U.S patent application no. 10/618,824, filed July 14, 2003.

Amend the following paragraphs in the specification as shown:

[0012] Figure ~~1a~~ 1A is a cross section of a partially fabricated programmable conductor memory cell in an integrated circuit, constructed in accordance with a preferred embodiment of the present invention.

[0013] Figure ~~1b~~ 1B is a perspective view of the partially fabricated programmable conductor memory cell of Figure ~~1a~~ 1A.

[0014] Figure ~~1c~~ 1C is a cross section of a partially fabricated memory cell for ~~and~~ an integrated circuit, constructed in accordance with another embodiment of the present invention.

[0016] Figure 3 is a cross section showing the programmable conductor memory cell of Figure 1~~a~~A after deposition of an insulating layer, formation of an anode via therein and deposition of conformal layer of silicon nitride, according to another embodiment of the current invention.

[0021] For example, the interface between the cell body sidewall and the surrounding insulating layer can provide a diffusion path for metal atoms and ions. When a metal anode layer (e.g., silver) is in contact with the edge (shown in Figure 1~~b~~B as 115) of the cell body sidewall, i.e., where the sidewall makes contact with the anode surface, there is additional diffusion of metal cations along the sidewall, through the interface, to the growing conductive pathway. If the anode via is designed to have the same width as the cell body via, even slight variations in mask registration can result in large differences in the

contact area between the anode and the edge of the cell body sidewall, regardless of conventional mechanisms to minimize the effect of mask misalignment. These differences in contact area lead to differences in the metal supply through the cell body/insulator interface to the growing conductive pathway. Thus, the extent of the conductive pathway formation would depend not just on applied voltage and/or switching time, but also on the amount of meal leakage along the sidewall. Accordingly, the preferred embodiments provide means for avoiding differential contact area between the anode and the edge of the glass electrolyte element.

[0022] A preferred embodiment of the current invention can be described beginning with reference to Figure ~~1a~~ 1A, wherein the first components of a simplified programmable conductor memory cell for an integrated circuit are shown. A cathode layer 101, which is connected to the negative pole of a power supply, is shown. Preferably, the cathode layer 101 comprises tungsten (W). An insulating layer 103, preferably silicon nitride (Si_3N_4) is deposited over the cathode layer 101. In other arrangements, it will be understood that the thick planarized insulating layer 103 can comprise a form of silicon oxide, such as TEOS or BPSG, although it is preferred to define the sidewall with a material that prevents the diffusion of metal between devices. The thickness of the insulating layer 103 is preferably between about 10 nm and 200 nm, more preferably between about 25 nm and 100 nm and most preferably about 50 nm. A cell body via 105 is etched through the insulating layer 103, opening a window to the cathode layer 101, using standard patterning and etching techniques. The width of the cell body via 105 is preferably between about 100 nm and 500 nm, more preferably between about 200 nm and 300 nm, and most preferably about 250 nm. The cell body via 105 is filled with a glass electrolyte 107 (sometimes referred to in the literature as a Glass Fast Ion Diffusion or GFID element). The illustrated cell body preferably includes a chalcogenide glass, more preferably a glass comprising germanium and selenium (Ge-Se) and most preferably, Ge_4Se_6, Ge_3Se_7 or Ge_2Se_8, and additionally includes metal ions. The actual ratios of elements in the cell body 107 can vary and more complicated structures for the cell body 107 and are also contemplated, one of which is illustrated in Figure ~~1e~~ 1C and discussed

below. Once the cell body via 105 is filled, the top surface 109 of the Ge-Se 107 is made level with the top surface 111 of the insulating layer 103, preferably by chemical mechanical planarization. Preferably the height of the programmable conductor memory cell body between the cathode surface and the anode surface is in the range of about 25 nm to 100 nm.

[0023] Some aspects of the glass electrolyte element that are helpful for understanding the embodiments of the current invention are shown in Figure ~~1b~~ 1B, a perspective view of the first components of the programmable conductor memory cell already seen in cross section in Figure 1A. The glass electrolyte element 107 is shown embedded in the insulating layer 103 and making contact with an underlying cathode layer 101. The sidewall 113 of the glass electrolyte element is defined as the outer, cylindrical (in the illustrated embodiment) surface of the element, which is defined by the surrounding via wall 105. The edge 115 of the sidewall 113 is the intersection of the glass electrolyte element sidewall 113 and the top surface 109. In the illustrated embodiment, the edge 115 of the sidewall 113 has the form of a circle.

[0026] Figure ~~1e~~ 1C illustrates another arrangement of the cell body 107, wherein like reference numerals are employed to refer to like parts among the different embodiments. In this arrangement, the cell body 107 includes three layers, comprising a first Ge-Se layer 107a (e.g., Ge_4Se_6). The skilled element artisan will appreciate that the embodiments discussed below are equally applicable to forming electrodes over the cell body 107 of Figure ~~1a~~ 1A, Figure ~~1b~~ 1B or of any of a variety of other programmable conductor arrangements. In the illustrated embodiment of Figure ~~1e~~ 1C, the intermediate layer 107b provides metal to the cell body 107 for formation of conductive pathways under the influence of applied electrical fields. The structure can be formed by blanket deposition and etch or by first forming and then filling a via. In either case, the sidewall of the insulator surrounding the cell body is referred to as a "via" herein.

[0033] Next, as shown in Figure 5, a metal anode layer 133, preferably including a metal or combination of metals from Group IB or Group IIB, more preferably

copper or zinc and most preferably silver, is deposited. Preferably, the metal anode layer 133 is deposited so that it fills the anode via 123 and forms a portion 135 overlying the second insulating layer 121 all as one contiguous body of material. The ~~ovelying~~ overlying portion 135 is subsequently patterned and etched as desired, depending upon the circuit design of the memory array.

[0038] Thus, in one embodiment of the current invention, an anode via is made smaller than the cell body via so that the overlying insulator layer covers the cell body/insulator interface. The smaller anode vias are positioned so that their bottoms make contact only with the cell body and do not extend to the cell body/insulator interface. In another embodiment, a spacer prevents contact between the anode material and the cell body/insulator interface by covering the interface with spacer material near the outer edge of the anode via bottom. The preferred embodiments thus give reliable control to the spacing between the edge of the anode and the edge of the memory cell body or GFID material. These structures ensure that the anode cations that precipitate out to form the conductive path are those that were intentionally and controllably ~~provide~~ provided to the glass electrolyte material, whether by photodissolution, separate ~~metal-contining~~ metal-containing layer (see Figure 1eC), co-deposition or any other manner of metal doping. Silver content dissolved within a GeSe glass, for example, is self limiting at about 30 atm %, thus providing a reliably consistent source of diffusion ions for selectively forming the conductive path. For a given cation (e.g., Ag) concentration in solution, this provides conductive pathway formation reproducibly dependent upon voltage applied across the electrodes and/or switching time.